IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) An article comprising:

a wire-bonding mounting substrate including an upper protective layer and a lower protective layer;

a first wire-bond pad disposed upon the upper protective layer; ~~and~~

a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; and

an interconnect filling the via.

2. (Previously Presented) An article comprising:

a wire-bonding mounting substrate including an upper protective layer and a lower protective layer;

a first wire-bond pad disposed upon the upper protective layer; and

a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad, wherein the wire-bonding mounting substrate includes a first edge, the article further including:

a second wire-bond pad disposed upon the upper protective layer;

a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; and

wherein the first via and the second via are staggered with respect to the first edge of the wire-bonding mounting substrate.

3-5. (Canceled).

6. (Original) The article of claim 1, wherein the wire-bond pad includes a first layer and a second layer, wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof.

7. (Previously Presented) The article of claim 1, wherein the wire-bond pad includes a first layer and a second layer, and wherein the second layer is one of identical material to the first layer, or at least one of a more noble, or a softer metal than the first layer.

8. (Currently amended) A package comprising:

a wire-bonding mounting substrate including an upper protective layer and a lower protective layer;

a first wire-bond pad disposed upon the upper protective layer;

a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad;

an interconnect filling the first via;

a die disposed above the upper protective layer; and

a first wire bond that couples the die to the first wire-bond pad.

9. (Previously Presented) The package of claim 8, further including:

a second wire-bond pad disposed upon the upper protective layer;

a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad.

10. (Previously Presented) The package of claim 8 further including:

a second wire-bond pad disposed upon the upper protective layer;

a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad;

a second bond wire that couples the die to the second wire-bond pad; and

wherein the respective lengths of the first bond wire and the second bond wire are adjusted so as to tune the package.

11. (Original) The package of claim 8, further including:

a first bump coupled to the first via.

12. (Original) The package of claim 8, further including:

a first bump coupled to the first via; and

a first trace that makes an electrical contact to the first bump.

13. (Original) The package of claim 8, further including:

a first bump coupled to the first via; and

a larger substrate coupled to the first bump.

14. (Original) The package of claim 8, wherein the first wire-bond pad is part of a plurality of wire-bond pads, and wherein each wire-bond pad is directly above a corresponding via from a plurality of vias.

15. (Original) The package of claim 8, wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, and wherein each via is coupled to a bump.

16. (Original) The package of claim 8, wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, wherein each via is coupled to a bump, and wherein each bump is directly below a corresponding via.

17. (Currently amended) A process comprising:

forming a first via in a wire-bonding mounting substrate, wherein the wire-bonding mounting substrate includes an upper protective layer and a lower protective layer, and wherein forming proceeds from the lower protective layer toward the upper protective layer; and

patterning a first wire-bond pad symmetrically and directly over the first via, wherein forming ceases upon contact with the first wire-bond pad.

18. (Canceled).

19. (Original) The process of claim 17, further including:
forming a via liner in the first via.

20. (Original) The process of claim 17, further including:
filling the first via with an interconnect.

21. (Original) The process of claim 17, wherein forming the first via precedes patterning the first wire-bond pad.

22. (Original) The process of claim 17, further including:
filling the first via with an interconnect;

coupling the first via to a first bump.

23. (Original) The process of claim 17, further including:
coupling the first wire-bond pad to a first bump.

24. (Currently amended) A method comprising:
forming a first via in a wire-bonding mounting substrate, wherein the wire-bonding mounting substrate includes an upper protective layer and a lower protective layer, and wherein forming proceeds from the lower protective layer toward the upper protective layer;
patterning a first wire-bond pad directly over the first via, wherein forming ceases upon contact with the first wire-bond pad; and
coupling a die to the first wire-bond pad.

25. (Original) The method of claim 24, further including:
forming a second via in the wire-bonding mounting substrate;
patterning a second wire-bond pad directly over the second via; and
coupling the die to the second wire-bond pad.

26. (Original) The method of claim 24, further including:
filling the first via with an interconnect.

27. (Original) The method of claim 24, further including:
filling the first via with an interconnect; and
coupling the first via to a first bump.

28. (Currently Amended) A computing system comprising:
a wire-bonding mounting substrate including an upper protective layer and a lower protective layer;
a first wire-bond pad disposed upon the upper protective layer;

a first via in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, wherein the first via includes a liner that is electrically conductive, wherein the first via penetrates the upper protective layer and the lower protective layer, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad;

a die disposed on the upper protective layer; and

dynamic random-access memory coupled to the die.

29. (Original) The computing system of claim 28, wherein the computing system is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

30. (Original) The computing system of claim 28, wherein the die is selected from a data storage device, a digital signal processor, a micro controller, an application specific integrated circuit, and a microprocessor.